A novel tensile Si (n) and compressive SiGe (p) dual-channel CMOS FinFET co-integration scheme for 5nm logic applications and beyond

Dong-il Bae, Geumjong Bae, Krishna K Bhuwalka, Seung-Hun Lee, Myung-Geun Song, Taek-soo Jeon, Cheol Kim, Wookje Kim, Jaeyoung Park, Sunjung Kim, Uihui Kwon, Jongwook Jeon, Kab-Jin Nam, Sangwoo Lee, Sean Lian, Kang-ill Seo, Sun-Ghil Lee, Jae Hoo Park, Yeon-Cheol Heo, *Mark S. Rodder, *Jorge A. Kittl, Yihwan Kim, Kihyun Hwang, Dong-Won Kim, Mong-song Liang and ES Jung

Samsung R&D Center, Samsung Electronics, Hwasung-City, Gyeonggi-Do, Republic of Korea,
*Advanced Logic Labs, 12100 Samsung Blvd, Austin, TX, USA, email: equal72@samsung.com

Abstract— A novel tensile Si (tSi) and compressive SiGe (cSiGe) dual-channel FinFET CMOS co-integration scheme, aimed at logic applications for the 5nm technology node and beyond, is demonstrated for the first time, showing electrical performance benefits and excellent co-integration feasibility. A Strain-Relaxed SiGe Buffer (SRB) layer is introduced as buried stressor and successfully transfers up to ~1 GPa uniaxial tensile and compressive stress to the Si/SiGe n-/p-channels simultaneously. As the result, both tSi and cSiGe devices show a 40% and 10% electron and hole mobility gain over unstrained Si, respectively. Through a novel gate stack solution including a common interfacial layer (IL), HK, and single metal gate for both n- and pFET, secured process margin for 5nm gate length, low interface trap density (Dit) for SiGe channel and threshold voltage (Vt) target for both the Si and SiGe device are successfully demonstrated. Lastly, reliability investigation shows that tSi and cSiGe, employing the newly developed common gate stack scheme, possess superior reliability characteristics compared with those of equivalent Si devices.

I. INTRODUCTION

CMOS logic technology, based on the conventional Si FinFET structure, will unescapably approach performance limitations at the 5nm technology node and beyond, due to the challenge of continuous physical scaling [1,2]. The introduction of new channel materials, together with the necessary strain engineering, represents an attractive option to boost the transistor channel mobility and, in turn, ensure continuous CMOS logic scaling [3,4]. SiGe recently emerged as a promising pFET channel alternative to Si due to both its superior hole mobility and mature processing in view of mass production [5]. Strain is traditionally acknowledged as mobility booster, having been already implemented in previous technology nodes in the form of embedded SiGe S/D (eSiGe) for Si pFETs [6-8]. On the other hand, little solution has been known for effective electron mobility booster, in the form of a tensile stressor for Si nFET. Therefore, the simultaneous implementation of tensile strain for Si n-channel, together with compressive strain for SiGe p-channel by replacing Si with SiGe, would be an attractive option to enable continuous performance improvement. However, issues such as threading dislocations density (TDD) of epi, gate stack engineering with extremely scaled gate length and the intrinsic difference between the processing requirements of Si and SiGe, emerge as severe co-integration challenges.

In this work, a novel dual channel CMOS scheme has been demonstrated within the framework of a VLSI fabrication standard, introducing both tensile stress for the Si nFET and compressive stress for the SiGe pFET, whereby SiGe replaces the conventionally employed Si channel. A buried SRB global stressor is employed to induce tensile and compressive strain for nFET and pFET, respectively, resulting in electrical performance gain. Device impact of TDD induced by SRB is carefully confirmed by SRAM yield and leakage. The use of a novel CMOS co-integration scheme, which employs common IL, HK and a single WFM, helps achieving the Vt targets required for both nFET and pFET at extremely scaled gate lengths. The enhanced performance and the reliable gate stack demonstrated the suitability of the integration scheme developed in this work for logic applications for the 5nm logic technology node and beyond.

II. DEVICE DESIGN AND FABRICATION

A. Device design

Fig. 1(a) illustrates the tSi/cSiGe-channel CMOS device design with a global buried SiGe SRB stressor and a common gate stack (MG/HK/IL). A comprehensive TCAD simulation was carried out to evaluate the strain induced by the SRB stressor, as shown in Fig. 1(b). A ~1 GPa tensile and compressive stress are predicted, respectively for nFET and pFET, including the use of an eSiGe stressor. Figs. 2(a,b,c) show the corresponding predicted channel mobility enhancement in tSi and cSiGe of 40% (electron mobility) and 60% (hole mobility), respectively.

B. Device integration

Fig.3 is describing key steps of the CMOS co-integration process flow using tensile Si and compressive SiGe fin profiles. Fig. 4 summarizes the progress in SiGe SRB epitaxy development, showing that the initially high TDD is significantly reduced to ~5E4 cm^{-2} after optimization of both the thickness and arrangement of the intermediate SiGe buffer

layers. A 128M Si FinFET SRAM array was fabricated with 2.3E5cm^{-2} TDD to evaluate the impact of underlying defects on circuit operation in Fig. 5. Results show that Vmax/Vmin yield and leakage levels are comparable with those of a reference SRAM structure (on bulk Si). Si channel in pFET region is replaced by SiGe by epitaxy to implement the compressive strain and Vt tuning with single WFM. A novel STI process scheme has been developed in order to protect both the SiGe channel and the SRB from the detrimental effects of oxidation. Another challenge is represented by the variation of Ge content in the SiGe channel, as shown in Fig. 6. An increase of Ge content results in both a degradation of Dit and a shift of Vt. After reducing the burden of thermal treatment in oxidant and ambient atmosphere, the SiGe epitaxy process control has been improved so that the difference in Ge content between fin center and edge is less than 4% [Fig. 7].

C. Strain analysis:

A Geographic Phase Analysis (GPA) has been used to map the lattice constant (i.e., strain) of Si and SiGe channels. Fig. 8(a) shows a map of lattice strain ε_{xx} and ε_{yy} along the fin X- and Y- directions, respectively. The X-cut shows that the Si channel strain ε_{xx} is almost matched to that of the SiGe SRB, indicating tensile strain along the Si fin. On the other hand, the Y-cut shows that the Si channel strain ε_{yy} is almost matched to that of the Si substrate, confirming almost fully relaxed strain in the direction perpendicular to the Si fin. Fig. 8(b) shows the lattice mismatch to (unstrained Si) profile along the fin depth. Similarly, uniaxial compressive strain along the fin direction is observed for the cSiGe channel device, as well. The evolution of the channel stress during processing is shown in Fig. 9. A relative tensile stress clearly shows elastic stress relaxation after S/D recess process. After optimization of the S/D recess, around ~1GPa tensile and compressive stress were recovered by employing a non-recessed SD scheme for the nFET, and an embedded SiGe scheme for the pFET.

III. Electrical results

Fig. 10 (a) shows the long channel electron mobility gain of 40% in tSi over unstrained Si. The I_{soff}-I_{eff} plot in Fig. 10(b) confirms a remarkable ~14% short channel DC performance gain over an equivalent unstrained Si nFET. I_D-V_G characterization of the tSi devices fabricated demonstrates better current drivability than unstrained Si devices and comparable short channel characteristics [Fig. 11(a)]. A Vt lowering due to band gap narrowing is also observed in Fig. 11(b), further proving the successful application of stress engineering to the Si nFET.

The long channel performance of the cSiGe pFET has been analyzed and compared with that of an equivalent Si pFET, in order to quantify stress and mobility gain. The I_D-V_G plot in Fig. 12(a) illustrates the current gain and Vt shift of the SiGe channel. The G_m-V_G plot in Fig. 12(b) shows a transconductance gain of 10% over an equivalent Si pFET reference, even with 1 GPa compressive stress (as shown in Fig. 9). The reason for the lower mobility gain of the pFET is attributed to the Dit increase of the SiGe channel. Fig. 13 shows a clear degradation of SS and relative mobility due to increase of Dit. Extensive Dit improvement tests, focused on IL formation and pre/post-IL treatments, have been carried out in order to decrease Dit. Fig. 14 summarizes the results of Dit accumulated learning: although the achieved Dit is almost on target, further process optimization is needed to pursue the expected mobility gain.

The use of an extremely scaled gate length at the 5nm logic technology node forbids the securing of a conventional gate stack process window, which includes a different WFM for the n- and the pFET and additional metals for multiple Vt. Fig. 15 shows that a single WFM allows both the tSi and the cSiGe channel to achieve their Vt targets simultaneously, regardless of the Ge content. The gate stack scheme employed (common metal gate, HK, and IL) tremendously simplifies not only n/pFET co-integration flow, but also the quest for a multiple Vt scheme for the 5nm logic technology node.

Reliability has also been comprehensively investigated for both tSi and cSiGe channel devices. n-/pFET BTI reliability superior to that of the Si counterpart is demonstrated, as shown in Fig. 16. A robust negative gate bias temperature instability (NBTI) behavior has been achieved for cSiGe pFET, due to oxide electric field (E_{ox}) alleviated by negatively charged traps. The choice of SiGe as SRB material could, in principle, pose self-heating concerns, as SiGe is characterized by a thermal conductivity 20 times lower than that of Si [9]. Nevertheless, simulations confirm that, although the SiGe SRB layer is responsible for increased device temperature under DC operation, negligible AC performance degradation is observed thanks to the high frequency operation and thermal dissipation through the metal contacts [Fig. 17].

IV. Conclusions

In summary, a novel dual-channel CMOS FinFET scheme with tensile Si nFET and compressive SiGe pFET on a SiGe SRB stressor, aimed at 5nm and beyond logic applications, has been demonstrated for the first time. The results show excellent electrical performance gain and robust reliability characteristics over equivalent Si CMOS FinFET devices. Both gate scaling to 5nm-node lengths, and a reduction of the process complexity, have been achieved by using a common gate stack. Therefore, the co-integration of tSi and cSiGe on the same CMOS FinFET platform provides a promising path to pursue logic scaling to the 5nm tech. node and beyond.

Acknowledgements

The authors gratefully acknowledge the contribution of the Joint Development Alliance with IBM and Global Foundries for the insightful technical discussion and valuable output of the cooperative partnership.

References

[1] R. Chau et al., IEEE Trans on Nanotech.,2005, vol.4, P.153. [2] K. J. Kuhn et al., IEDM, 2012, P.8.1.1. [3] S. Datta et al., IEDM, 2003, P.28.1.1. [4] R. Pillarisetty et al., IEDM, 2010, P.6.7.1 [5] S. Krishnan et al., IEDM, 2011, P.28.1.1 [6] S. Thompson et al., IEDM, 2002, P.61. [7] T. Ghani et al., IEDM, 2003, P.11.6.1. [8] S. Tyagi et al., IEDM, 2005, P.245. [9] K. A. Jenkins et al., EDL, 23(6), P.360, 2002.

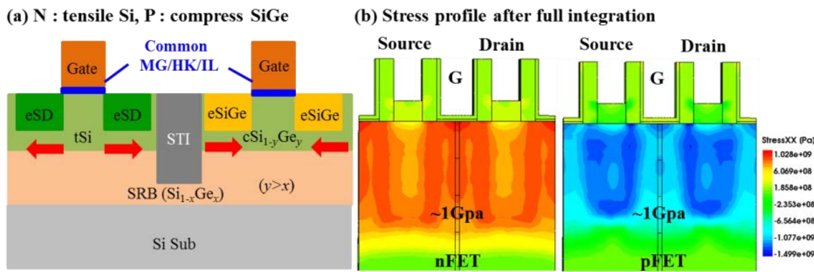

Fig. 1(a). CMOS design concepts for logic 5nm and beyond application: SiGe SRB as global stressor for both Si channel nFET and SiGe channel pFET. (b) TCAD simulation indicates that SRB stressor can transfer over 1 GPa tensile stress for nFET and compressive stress (including eSiGe stressor) for pFET.

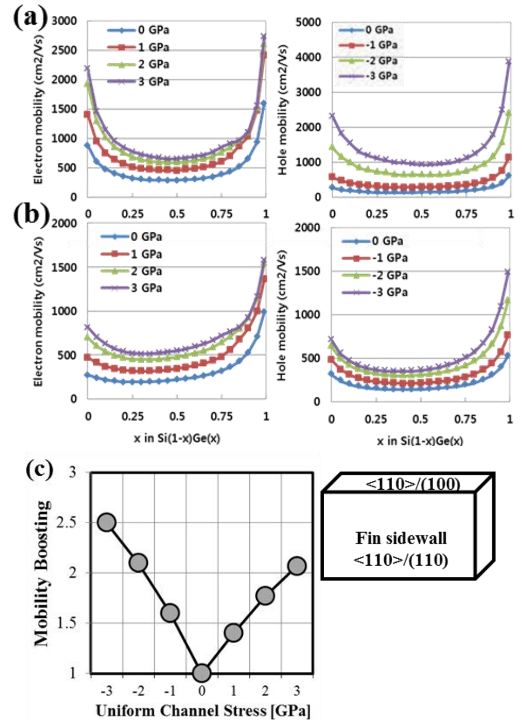

Fig. 2 (a) <110>/(110) (b) <110>/(100) TCAD simulation shows SiGe bulk mobility (considering alloy scattering) dependence on Ge content and stress (c) tSi and cSiGe show mobility gain of 40% and 60% at stress of 1 GPa, respectively.

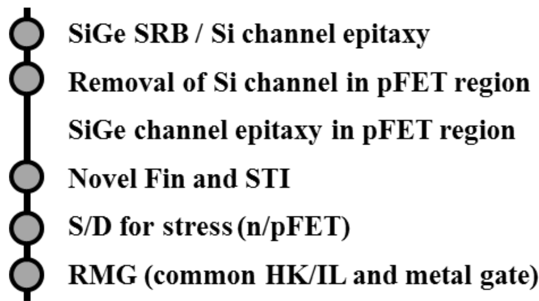

Fig. 3. Key steps to enable tSi/cSiGe CMOS, including new SiGe EPI, pFET SiGe replacement, novel STI, S/D engineering for stress and common RMG process considering both Si/SiGe channel.

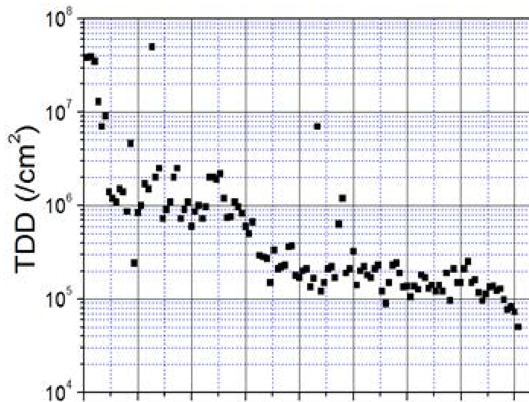

Fig. 4. SiGe SRB TDD reduced by buffer layer structure evolution and lowest TDD of 5E4 cm^{-2} achieved in this work.

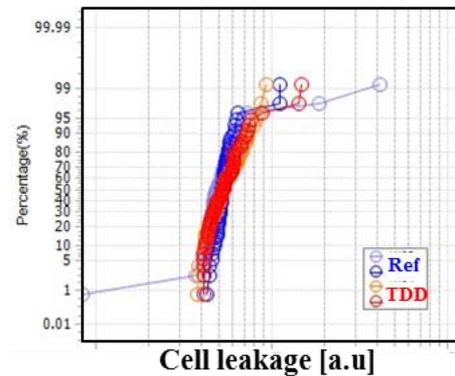

Fig. 5. 128M SRAM FinFET strucuture with TDD 2.3e5 cm^{-2} shows comparable yield and leakage with reference SRAM.

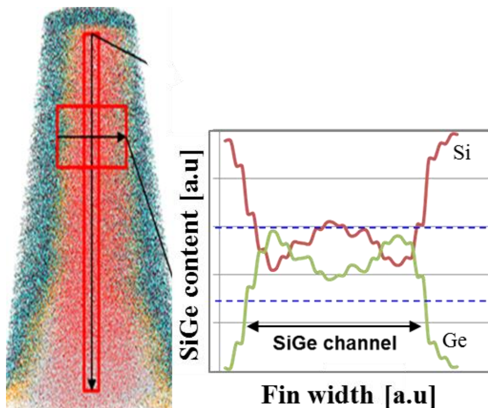

Fig. 6 Ge concentration profile in cSiGe fin. The surface shows higher Ge content than center because of subsequent thermal process

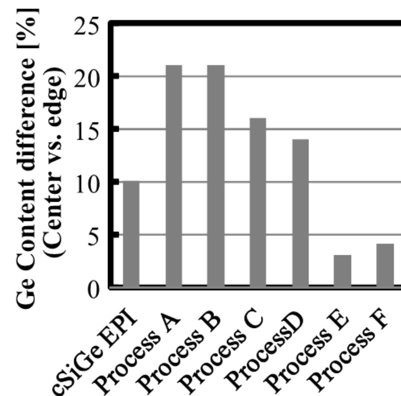

Fig.7. The Ge content can be well controlled (<4% center/edge difference) during processing by optimization.

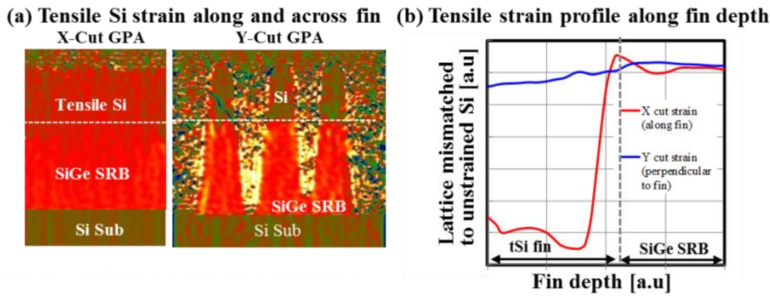

Fig. 8 (a) Geographic phase analysis (GPA) was used to capture the lattice information after fin etch. It shows clearly that uniaxial (along fin) tensile strain induced by SRB. Strain fully relaxed in the direction of perpendicular to fin. (b) Strain profile along fin depth shows uniaxial strain along fin but almost fully relaxed strain across fin.

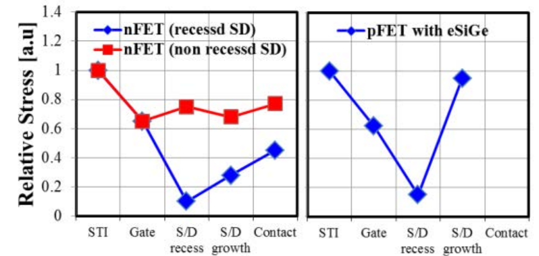

Fig. 9. N/PFET channel average stress evolution during processing. Relative tensile strain clearly shows elastic strain relaxation by source-drain recess process. After S/D recess optimization, strain relaxation has been minimized for the NFET and recovered with eSiGe process.

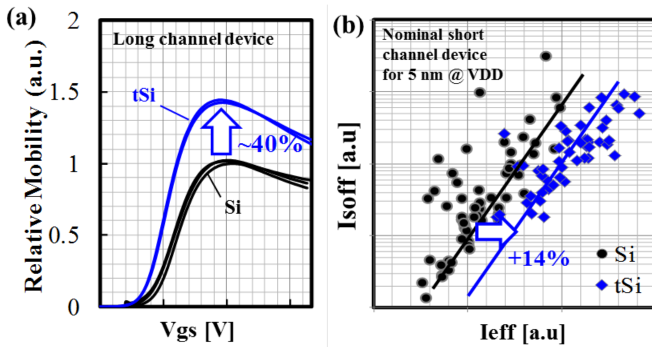

Fig. 10 (a) tSi shows ~40% higher electron mobility obtained from long channel device compared to Si reference. (b) Short channel I_{soff} vs. I_{eff} plot indicates ~14% Ieff performance gain over unstrained Si.

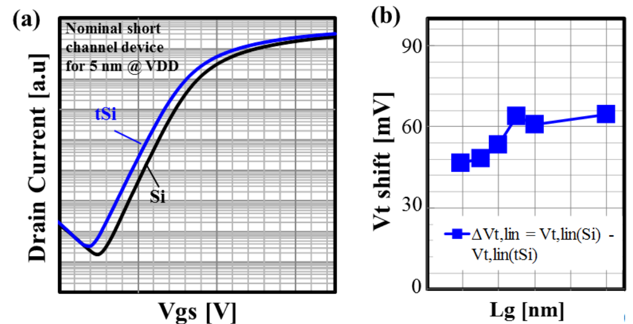

Fig. 11 (a) Short channel I_{soff} vs. I_{drain} plot indicates tSi has similar short channel characteristics and clear Vth shift by stress. (b) Vt lowering of ~60 mV is observed due to strain-induced Eg narrowing at all gate length.

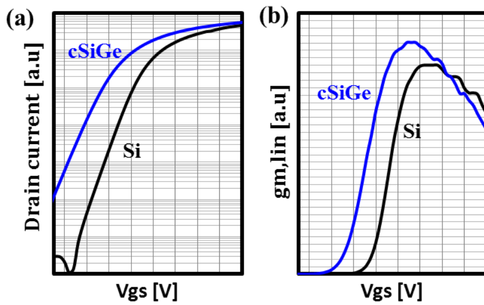

Fig. 12 (a) Id-Vg shows Vth shift and current gain by SiGe channel. (b) long channel SiGe device shows 10% better Gm than Si reference by compressive strain.

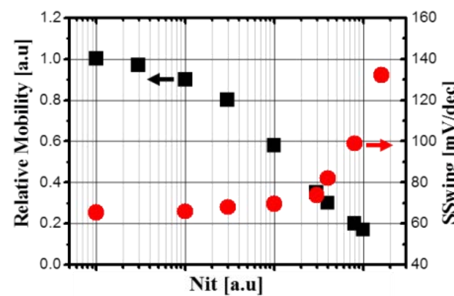

Fig. 13 Mobility and SS degradation due to Nit increase. SiGe channel shows clear performance degradation due to Dit increase. Dit control is the key process for SiGe channel performance.

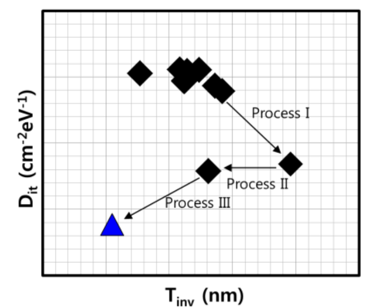

Fig. 14 Dit was significantly improved by novel pre-HK/IL, post-HK/IL treatment. Several splits have been performed in order to achieve the target Dit and Tinv.

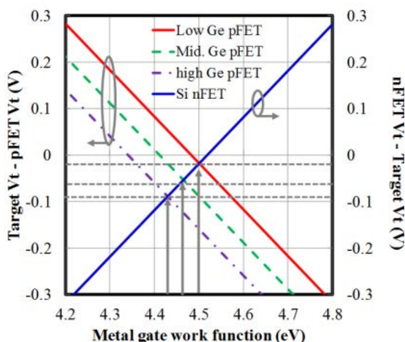

Fig. 15 Si nFET and SiGe pFET allow single WMF for Vt targeting, greatly simplifying the multi-Vt scheme.

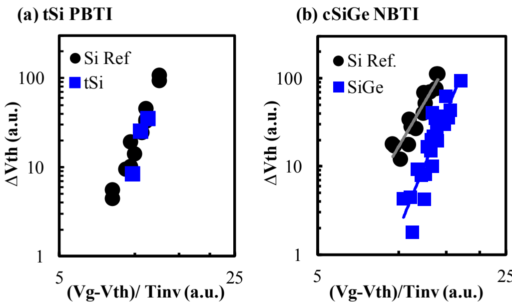

Fig. 16 (a) tSi shows PBTI comparable to that of a Si nFET and (b) cSiGe shows a more robust NBTI compared with that of a Si pFET.

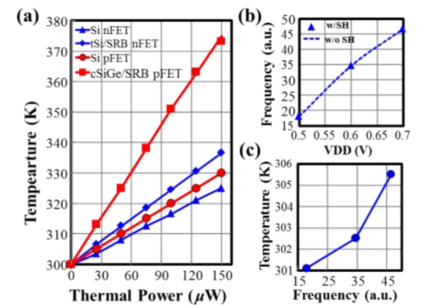

Fig.17 (a) Self-heating causes a temperature rise under DC operation but (b) and (c) show neglegible self-heating penalty under AC operation.